# Best Practices for PCB Design for SCNC19 Competitors

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**Introduction:**

There are many best practices that companies and individuals follow when designing PCBs (Printed Circuit Boards). We have researched best practices related to PCB layout and have compiled them here to help Experts train their competitors and during judging at the competition.

World Skills competitors are not considered to be experts in HF PCB design and as such these guidelines will focus on best practices to minimize noise radiation and reception and easing manufacture of circuits.

These best practices also are limited to single layer PCB design prototyped on an LPKF PCB Milling Machine. It is important to note that the techniques applied to PCBs manufactured by professional PCB factories may be very different from techniques needed when prototyping a milled board.

At the competition, techniques that are used should favour creating milled boards. This means spacing between traces may be larger than spacing used for factory produced boards. PCBs may need keepout areas so that the likelihood of shorts will be minimized. And Competitors should try to minimize the amount of rubout areas needed.

Otherwise if possible competitors should layout their boards as if they would be professionally manufactured. If there is a conflict choosing a technique that favours manufactured boards or milled prototype boards, the competitor should choose the technique that favours prototype boards.

While we do not expect competitors to know HF layout and EMC reduction techniques, we do expect they will follow these guidelines that minimize EMC radiation and follow HF rules.

When through hole was the dominant component packing method there were two layers; component side and solder side and this has evolved to multi-layer boards populated with SMD components. But in our competition currently, we can only make single-sided PCBs.

Therefore, this document will reflect best practice for single layer proto-type boards.

**Best Practices:**

1. In single layer PC boards all SMD components should be placed on the Bottom layer and all TH components should be placed on the Top layer

2. Power supply and other high current traces should be larger than signal traces. The rails should at a minimum be able to handle the current through them according to IPC-2152. A good guideline is:

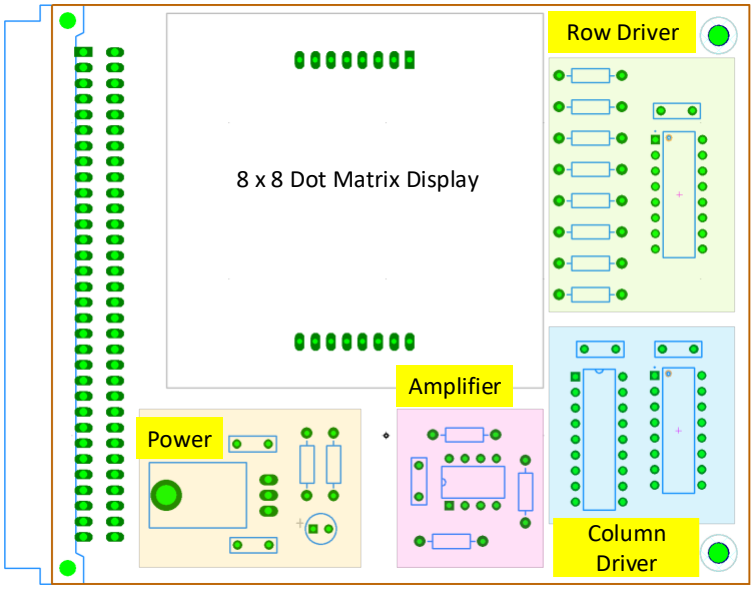
| | |
|---|---|
| 10 mils (0.25 mm) | 0.3 Amps |
| 16 mils (0.4mm) | 0.4 Amps |
| 20 mils (0.5mm) | 0.7 Amps |
| 24 mils (0.6mm) | 1.0 Amps |
| 50 mils (1.3 mm) | 2.0 Amps |
| 100 mils (2.5mm) | 4.0 Amps |
| 150mils (4 mm) | 6.0 Amps |

3. Signal traces should be as short as possible.

4. When beginning any layout, the components that must in a precise location have to be placed first. For example mounting holes, switches, LEDs and displays.

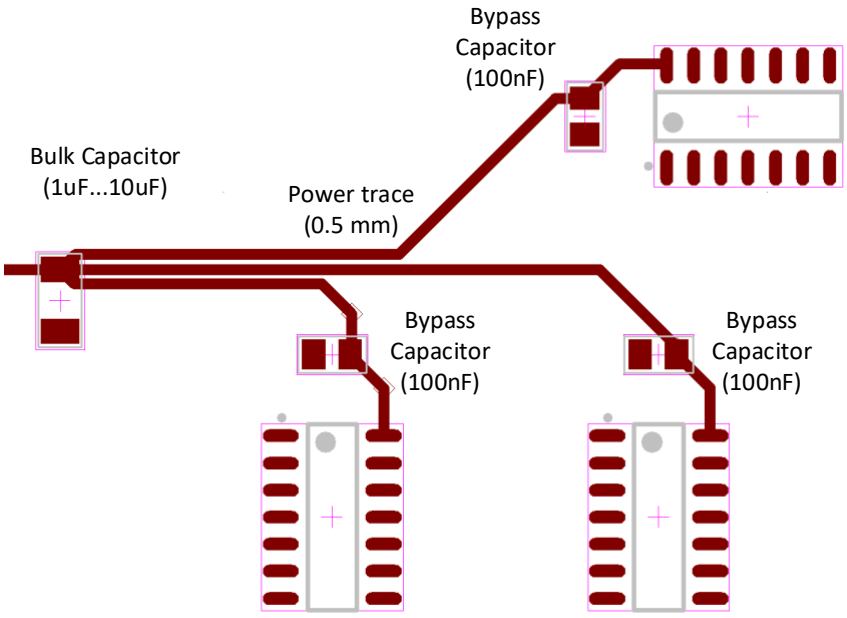
5. Make sure that temperature sensitive devices (like Electolytic caps, temperature sensors, etc) are separated from heat producing components.

6. Next, components should be grouped together in a logical way by function**. Poor grouping results in long traces, difficulty in routing and a poor PC board.**

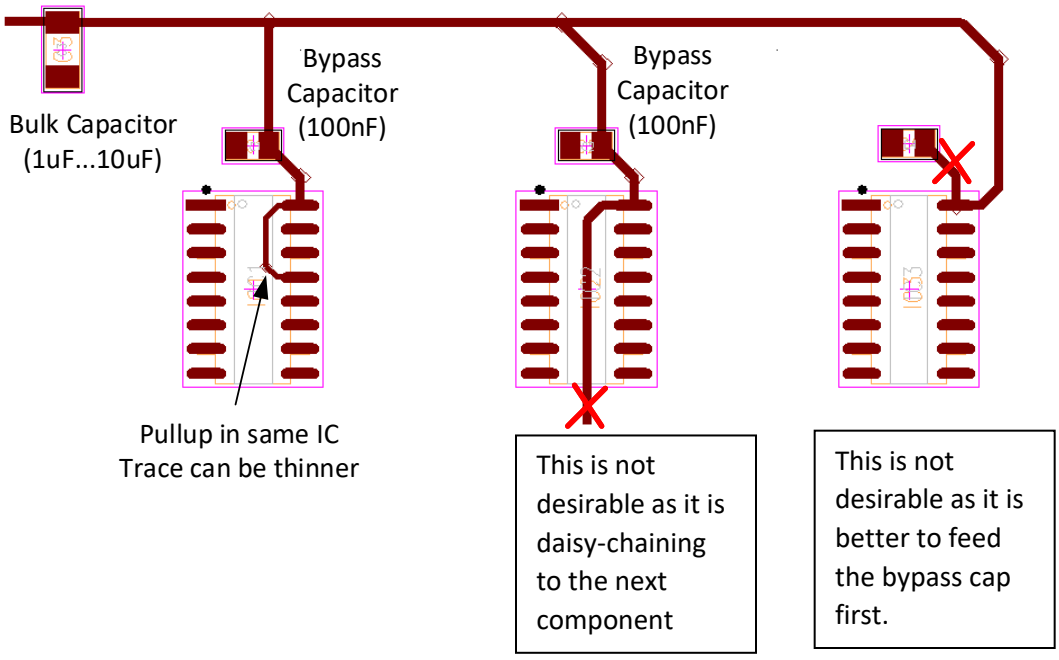



7. Try to separate areas that produce strong EM fields from circuits that may be sensitive to them.

8. Ideally, avoid daisy-chaining grounds and supply rails. Instead try to radiate power outwards from a central single point.




However, with single layer PCBs it isn't usually possible to do that way. We can accept stubs from a power rail.


Bulk Capacitor
(1uF...10uF)
Bypass
Capacitor
(100nF)
Bypass
Capacitor
(100nF)
Pullup in same IC
Trace can be thinner
This is not desirable as it is daisy-chaining to the next component
This is not desirable as it is better to feed the bypass cap first.

9. Use a ground plane to minimize noise radiation. Sometimes it is better to keep analog and digital grounds separate and connect them later at one point.

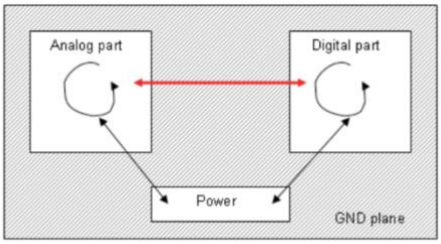
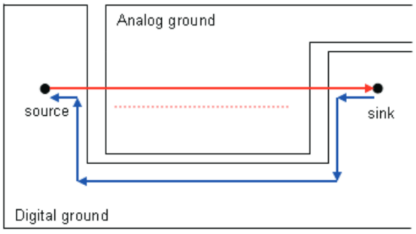


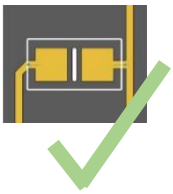

**Figure 9. Good Placement of Different Functional Blocks Without the Need of a Split Ground Plane**

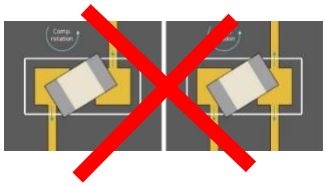
Sometimes it is not a good idea to separate ground planes. Here there is a large loop that will radiate.




If separate grounds are used, it is best to connect them at one point as close to the power return as possible.

10. Strive to give both side of component pads the same thermal load to minimize tombstoning and misaligned components.





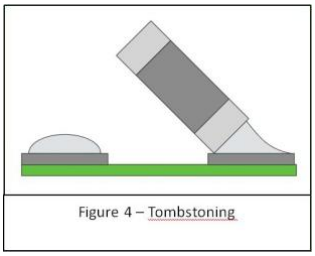
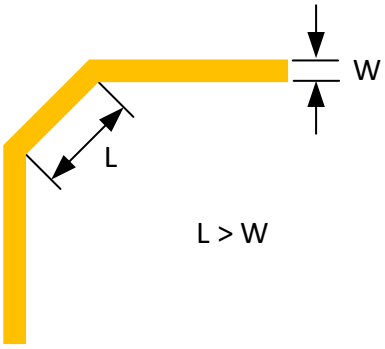


Figure 4 – Tombstoning

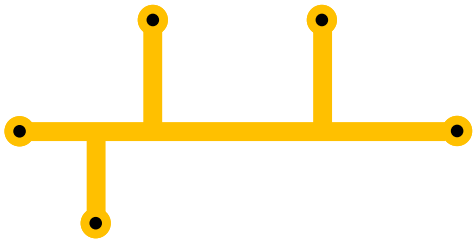
11. Use thermal reliefs for connections to large copper areas.


12. Use mitred or rounded corners so noise is minimized. (Does not apply to T intersections).

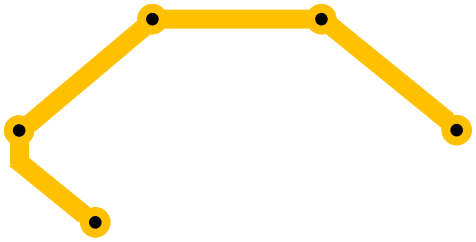
Sharp angle can cause noise injection into other tracks on the PCB. Therefore all corners should be rounded or mitred (angled) by 45 deg.



13. Avoid stubs with tracks carrying high frequency and sensitive signals (low voltage) because stubs produce reflections. Power lines stub are OK.

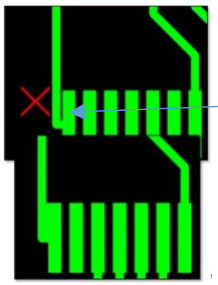


Connection via stub lines



Connection via continuous trace

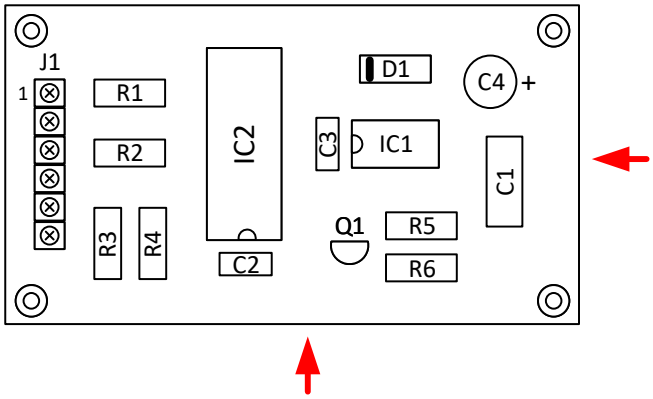
14. Avoid acid traps



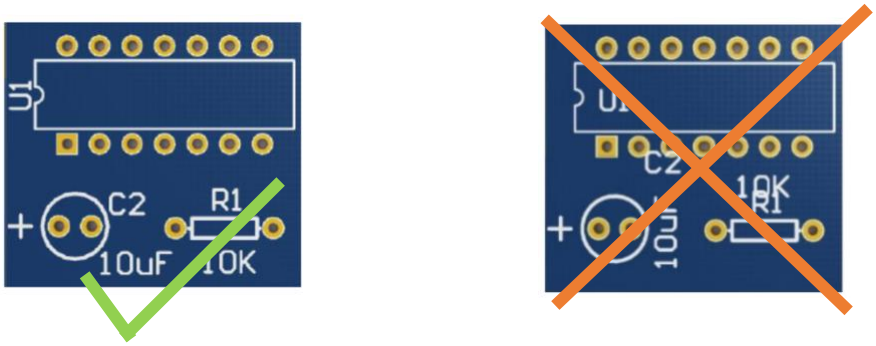
This space is small and etchant may collect here.

15. While we cannot produce a silk screen layer on our milled boards, Competitors should ensure reference designators and other needed information is present in the assembly documentation. All text should be in the same direction, ideally. There may be times where space does not permit this, and in this case the competitor should place the designation in a location that most clearly identifies where the component is located, or other important information related to the component.

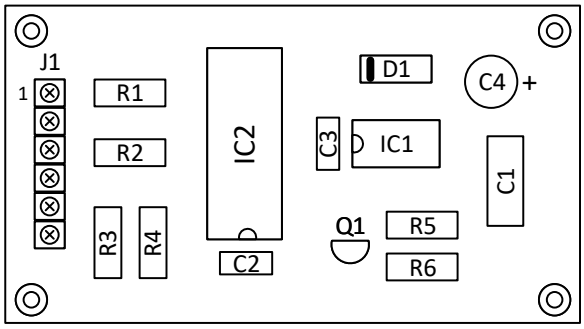
    Text should be readable in two directions only.




16. There should be no overlap of text onto other text or outlines.



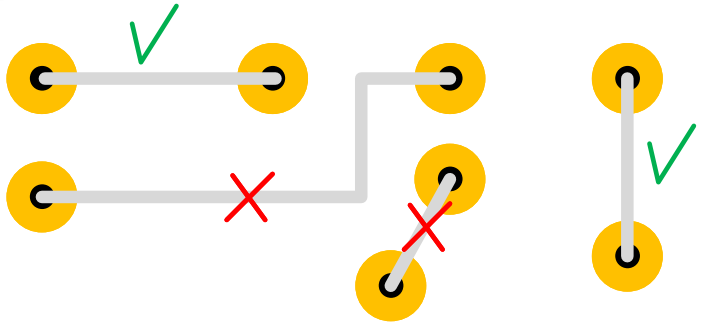

17. Polarized or Orientation Component Marking
    Components that have a polarity should be marked on the assembly documentation. Non-polarized components should also be indicated through markings on the assembly.




Notice that D1 and C4 show markings that indicate polarization. ICs show markings indicating orientation.

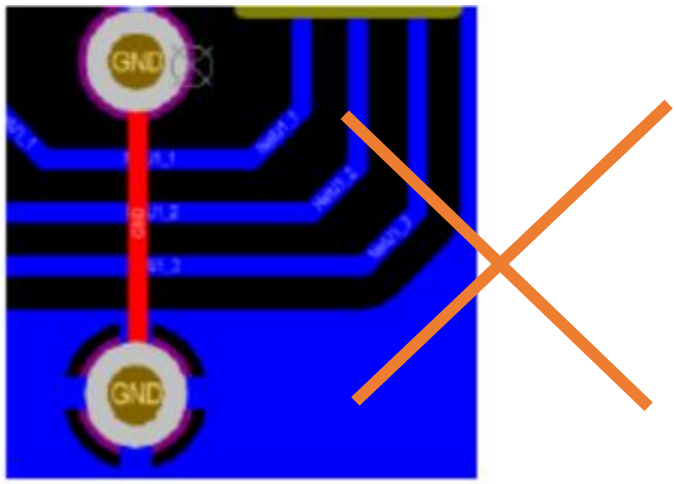
Resistors have no marking indicating orientation or polarization.

18. Jumper Wires

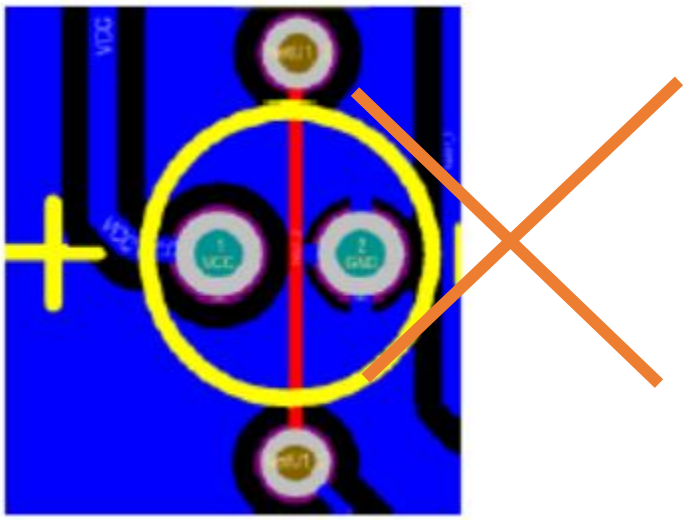


Jumper wires should be short, straight and not diagonal or crooked.

19. Jumpers to ground should be avoided. Grounds should be a continuous plane and adding wire jumpers adds an inductance in series with the ground.




20. Do not place jumpers under components.

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EMC at component and PCB level, Martin O'Hara